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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/008,270	**Applicant(s)** CAVANAGH ET AL.	
	Examiner Jason Proctor	**Art Unit** 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-17 and 20-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-17 and 20-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *7/25/05,10/17/05*.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

In view of the appeal brief filed on 14 November 2005, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Claims 1-6, 9-17, and 20-35 are pending in this application. Claims 1-6, 9-17, and 20-35 have been rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 28 and 29 are rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,881,267 to Dearth et al. ("Dearth").

Regarding claim 28, Dearth discloses a distributed simulator system (abstract) that counts a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator and to cause the cycle-based simulator to evaluate in response thereto [*"After a delay 712 (FIG. 7) after rising edge 710 of simulated clock signal CLOCK, i.e., at resolve time 702A, posting by VBS 114A (FIG. 4) is initiated. By delaying a period of time from the rising edge of the clock signal represented by clock 504 (FIG. 5), the state of bus 214 (FIG. 2) is resolved at a simulated time at which bus 214 should have a steady state."* (column 10, lines 31-44)]. Although Dearth does not recite *verbatim* "counting a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator," Dearth's simulator 116A is a clocked computer simulation system and therefore operates according to its computer clock cycles. "Delaying" the simulation clock signal represented by clock 504 is inherently a delay "equal to a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator." The only way for Dearth's simulator to perform such a delay is to count a number of timesteps (computer clock cycles) equal to the desired delay.

Regarding claim 29, Dearth discloses instructions executable to sample output signals of the model and drive input signals of the model [*"In FIG. 4, DSP 112A both drives and samples line 414 of bus 214 (FIG. 2)."* (column 8, lines 45-46); also (column 7, lines 1-19); *"VBS 114A stores in resolved output register 406 a simulated signal represented by the data received from resolved 302... VBS 114A drives the resolved signal on line 414 within simulation system 116A. In VBS 114A, the resolved signal stored in resolved output register 406 is applied to the input of output buffer 408."* (column 8, lines 26-44); etc.].

Claim Rejections - 35 USC § 103

The previous rejections under 35 U.S.C. § 103 have been withdrawn in response to Applicants' arguments.

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

2. Claims 1, 9-11, 12, 20-22, and 30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,881,267 to Dearth et al. ("Dearth") in view of US Patent No. 5,910,903 to Feinberg et al. ("Feinberg").

Regarding claim 1, Dearth teaches a distributed simulation system (FIG. 1) comprising:

A first node (FIG. 1, 100A) configured to simulate a first portion of a system under test (FIG. 1, 112A) using a first simulator program (FIG. 1, 116A);

A second node (FIG. 1, 100B) configured to simulate a second portion of a system under test (FIG. 1, 112B) using a second simulator program (FIG. 1, 116B);

[*"In this simple, illustrative example, DSPs 112A and 112B are distributed model parts and collectively simulate a complete, simulated circuit 200 (FIG. 2)."* (column 4, lines 37-39);

"Simulation system 116A can be, for example, the Cadence Verilog hardware simulator..." (column 6, lines 49-52)]

wherein the first node and second node communicate at least signal values during the simulation using message packets formatted according to a grammar [*"For example, simulation system 116B can transfer data to hub 110A by including computer instructions which, when executed by processor 102B, cause processor 102B to transfer the data,* ***including specification of hub 110A of computer 100A as the recipient of the data,*** *to network access device 120B and to issue control signals to network access device 120B* ***to send the data through network 130.*** *Network access device 120B, in response to the control signals, sends the data* ***to network 130, which forwards the data to computer 100A in accordance with the specification of the recipient.*** *Network access device 120A retrieves the data from network 130 and transfers the data to* ***processor 102A which then writes the data to hub 110A in accordance with the specification of the recipient. The transfer of data between computers 100A and 100B through network 130 is conventional and well-known."*** (column 6, lines 7-21, emphasis added); *"Since each of circuit parts 212A and 212B must adhere to the bus protocol implemented by bus 214, the bus protocol is an inherent part of the design of each of DSPs 112A (FIG. 1) and 112B."* (column 5, lines 18-22)];

and wherein a simulation of the system under test comprises a first node simulating the first portion of the system under test and the second simulating the second portion of the system under test [*"As a result, VBSs 114A and 114B collectively accurately simulate bus 214 (FIG. 2) which connects circuit parts 212A and 212B* [the real system under test] *which are in turn* *simulated by DSPs 112A (FIG. 1) and 112B, respectively* [the corresponding nodes simulating the first and second portions of the system under test]*"* (column 4, lines 54-57)];

and wherein the distributed simulation system further comprises a hub coupled to the first node and the second node (FIG. 3, 110A), wherein the hub is configured to route the message packets from the first node ot the second node and from the second node to the first node [*"With each simulated cycle of a clock of bus 214, a hub 110A (FIG. 1) (i) collects data which represents components of the simulated state of bus 204 (FIG. 2) from VBSs 114A (FIG. 1) and 114B, (ii) resolves the current simulated state of bus 214 (FIG. 2), and (iii) sends data representing the resolved state of the simulated bus to VBss 114A (FIG. 1) and 114B. As a result, VBSs 114A and 114B collectively accurately simulate bus 214 (FIG. 2) which connects circuit parts 212A and 212B which are in turn simulated by DSPs 112A (FIG. 1) and 112B, respectively."* (column 4, lines 48-57); *"Hub 110A can execute in a computer in which no other simulation systems execute."* (column 5, lines 3-5)].

Dearth does not expressly teach "the instruction code comprising the first simulator program differs from the instruction code comprising the second simulator program."

Feinberg teaches a distributed simulation (abstract) wherein the instruction code comprising a first simulator program differs from the instruction code comprising a second simulator program [*"In the example of FIG. 1,* ***simulation component A comprises a mock cockpit as its simulation processor 105*** *running software which simulates a plane as its simulation entity 130,* ***simulation component B comprises a black box which may be***

***constructed in any manner known to those skilled in the art** and depending upon the purpose of the simulation which is operatively connected to an actual tank where the tank is the simulation entity 130, and **simulation component C comprises a Sun workstation as the simulation processor 105** running a computer software model of a missile which model is the simulation entity 130, and **simulation component D comprises an Intel-based personal computer as the simulation processor 105** running a computer software model of a radar system as its simulation entity 130. As may be seen from the diagram, each of the simulation processors 105 are running DIS software 110 where the DIS software on each simulation component 100 passes a PDU 120 to each of the other simulation components 100."* (column 2, lines 1-18; emphasis added)].

Dearth and Feinberg are analogous art because they are both distributed simulation systems.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the different simulators in a distributed simulation of Feinberg in the distributed simulation of Dearth because Feinberg teaches that different simulators allows for broad flexibility in the simulation components; allows for using commercial off the shelf ("COTS"), government off the shelf ("GOTS"), or customized computer applications; and allows for implementing new data collection as required to react to new questions, new simulation objectives, new simulations, etc. (column 3, line 63 – column 4, line 5).

Regarding claim 9, Microsoft Computer Dictionary, Fifth Edition, defines **port** as:

> 1. An interface through which data is transferred between a computer and other devices (such as a printer, mouse, keyboard, or monitor), a network, or a direct connection to another computer. The port appears to the CPU as one or more memory addresses that it can use to send or receive data. Specialized hardware, such as in an add-on circuit board, places data from the device in the memory addresses and sends data from the memory addresses to the device. Ports may also be dedicated solely to input or to output. Ports typically accept a particular type of plug used for a specific purpose. For example, a serial data port, a keyboard, and a high-speed network port all use different connectors, so it's not possible to plug a cable into the wrong port. *Also called:* input/output port. 2. port number.

Dearth expressly discloses that the grammar includes a first command defining one or more logical ports and one or more logical signals [*"For example, simulation system 116B can* ***transfer data*** *to hub 110A* ***by including computer instructions*** *which, when executed by processor 102B, cause processor 102B to transfer the data,* ***including specification of hub 110A of computer 100A as the recipient of the data,*** *to network access device 120B and to issue control signals to network access device 120B to send the data through network 130...* ***The transfer of data between computers 100A and 100B through network 130 is conventional and well-known."*** (column 6, lines 7-21; emphasis added)].

Regarding claim 10, Dearth expressly teaches that the grammar includes a second command defining a mapping between the logical signals and physical signals of a model of each portion of the system under test [(column 6, lines 7-21); *"Since each of circuit parts 212A and 212B must adhere to the bus protocol implemented by bus 214* [the physical signals of the modeled system under test] *the bust protocol is an inherent part of the design of each of DSPs 112A (FIG. 1) and 112B."* (column 5, lines 18-22)]. The "mapping" between logical signals (*transmitted data*) and physical signals (*signals in the system under test*) is at least an inherent aspect of Dearth's distributed simulation system, where one DSP receives input signals and transmits output signals to a VSB representing the remainder of the circuit. (See also column 4, lines 48-67; alternatively column 6, lines 33-52).

Regarding claim 11, Dearth expressly teaches that the grammar includes a third command defining a routing between the logical ports of the portions of the system under test [*"For example, **simulation system 116B can transfer data to hub 110A** by including computer instructions which, when executed by processor 102B, cause processor 102B to transfer the data, including specification of hub 110A of computer 100A as the recipient of the data, **to network access device 120B and to issue control signals to network access device 120B to send the data through network 130... The transfer of data between computers 100A and 100B through network 130 is conventional and well-known.**"* (column 6, lines 7-21; emphasis added)].

Claims 12 and 20-22 recite the method performed by the system of claims 1 and 9-11 and are therefore rejected for the same rationale as claims 1 and 9-11.

Claim 30 recites a system that merely rephrases the limitations of claim 1 and is therefore rejected for the same rationale as claim 1.

3. Claims 2-3, 5-6, 13-14, 16-17, 31-32, and 34-35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dearth in view of Feinberg as applied to claim 1 above, and further in

view of "Handbook of Simulation" edited by Jerry Banks ("Banks", cited on PTO-892 of paper number 20050228 and provided with Non-Final Office Action of 9 March 2005).

Regarding claim 2, neither Dearth nor Feinberg expressly teach the use of event-based simulators, however Banks expressly teaches that event-based simulators are known in the prior art.

Regarding claim 3, neither Dearth nor Feinberg expressly teach that a first event-based simulator includes a first event scheduler which differs from a second event scheduler.

Banks expressly teaches an event-based simulation method (*discrete-event simulation model*) defined as "one in which the state variables change only at those discrete points in time at which events occur." (page 8, § 1.3.7 Discrete-Event Simulation Model) Banks further teaches the characteristics of a *discrete-event simulation model* [*"A discrete-event model attempts to represent the components of a system and their interactions to such an extent that the objectives of the study are met."* (page 6, § 1.3.1 System, Model, and Events); *"Discrete-event simulation models include a detailed representation of the actual internals. Discrete-event models are* dynamic*; that is, the passage of time plays a crucial role. Most mathematical and statistical models are* static*, in that they represent a system at a fixed point in time."* (page 7, § 1.3.1 System, Model, and Events)].

Banks expressly teaches "event-scheduling" (implicitly the "event scheduler" which performs the same) (page 9, § 1.4.2 Event Scheduling Method). An event scheduler is an inherent and required component of an event based simulator, and therefore each of Dearth's DSPs 112A, 112B, etc., inherently comprise a different event scheduler. However, in light of the specification, it seems likely that Applicants' use of the term "event scheduler" most accurately corresponds with the term "list processor" or "list processing" as known in the art. Banks expressly teaches list processing (page 8, § 1.3.5 List Processing):

> Entities are managed by allocating them to resources that provide service; by attaching them to event notices, thereby suspending their activity into the future; or by placing them into an ordered list. Lists are used to represent queues.
>
> Lists are often processed according to FIFO (first in, last out), but there are many other possibilities. For example, the list could be processed by LIFO (last in, first out), according to the value of an attribute, or randomly, to mention a few. An example where the value of an attribute may be important is in SPT (shortest process time) scheduling. In this case the processing time may be stored as an attribute of each entity. The entities are ordered according to the value of that attribute, with the lowest value at the head or front of the queue.

Therefore Banks expressly teaches different event schedulers (*list processors*) with corresponding advantages, such as FIFO which is clearly a simple, robust list processing scheme, or SPT which optimizes the processing time.

Banks and Dearth in view of Feinberg are analogous art because both directed to simulation systems.

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a discrete-event simulation model taught by Banks, a handbook of teachings well-known to those of ordinary skill in the art of simulation, in the distributed simulation system of Dearth in view of Feinberg because Banks expressly teaches that discrete-event simulation models include a detailed representation of the actual internals, which improve over a mathematical, statistical, or input-output model that represent the internals of the model only with mathematical or statistical relationships (Banks, pages 6-7, § 1.3.1 System, Model, and Events) and therefore enhance the adaptability and versatility of those models as well as enhance the ability to validate the model's operation.

Regarding claims 5 and 6, neither Dearth nor Feinberg expressly teach a first simulator program comprising an event-based simulator and a second simulator program comprising a cycle-based simulator. Neither Dearth nor Feinberg expressly teach that the second node (comprising a cycle-based simulator) is configured to count a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator and to cause the cycle-based simulator to evaluate in response thereto.

Regarding claim 5, the rejection of claims 1 and 2 are incorporated showing that it would have been obvious to a person of ordinary skill in the art at the time the invention was made (as per claim 1) to use different simulators in different nodes of a distributed simulation, and (as per claim 2) to use event-based simulators in the distributed simulation system of Dearth in view of Feinberg.

Further, Dearth expressly teaches using a cycle-based simulator [*"Simulated time is kept by simulation system 116A (FIG. 1) and represents time elapsing during operation of the circuit simulated by simulation system 116A... After a delay 712 (FIG. 7) after rising edge 710 of simulated clock signal CLOCK, i.e., at resolve time 702A, posting by VBS 114A (FIG. 4) is* *initiated.*" (column 10, lines 31-44); Simulation of a clock signal in a digital circuit constitutes a cycle-based simulation wherein the clock signals indicate the cycles of simulation.]

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Banks regarding an event-based simulation with the distributed simulation system of Dearth in view of Feinberg to create a distributed simulation system where a first node comprises an event-based simulator and a second-node comprises a cycle-based simulator for the reasons provided in the rejection of claim 1.

Regarding claim 6, Dearth teaches a cycle-based simulator that counts a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator and to cause the cycle-based simulator to evaluate in response thereto [*"After a delay 712 (FIG. 7) after rising edge 710 of simulated clock signal CLOCK, i.e., at resolve time 702A, posting by VBS 114A (FIG. 4) is initiated. By delaying a period of time from the rising edge of the clock signal represented by clock 504 (FIG. 5), the state of bus 214 (FIG. 2) is resolved at a simulated time at which bus 214 should have a steady state.*" (column 10, lines 31-44)]. Although Dearth does not recite *verbatim* "counting a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator," Dearth's simulator 116A is a clocked computer simulation system and therefore operates according to its computer clock cycles. "Delaying" the simulation clock signal represented by clock 504 is inherently a delay "equal to a number of timesteps equal to a number of timesteps per clock cycle of the clock corresponding to the cycle-based simulator."

Claims 13-14 and 15-16 recite the method performed by the system of claims 2-3 and 5-6 and are therefore rejected for the same rationale as claims 2-3 and 5-6.

Claims 31-32 and 34-35 recite a system that merely rephrases the limitations of claims 2-3 and 5-6, and are therefore rejected for the same rationale as claims 2-3 and 5-6.

4. Claims 4, 15, and 33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dearth in view of Feinberg in view of Banks as applied to claim 3 above, and further in view of "CSC1 320 Computer Architecture Handbook on Verilog HDL" by Dr. Daniel C. Hyde ("Hyde").

Regarding claim 4, none of Dearth, Feinberg, or Banks expressly teach a model comprising a non-blocking assignment, however Dearth does expressly teach that the simulators can be a Verilog hardware simulator [*"Simulation system 116A can be, for example, the Cadence Verilog hardware simulator... "* (column 6, lines 49-52)].

Hyde teaches the capabilities of the Verilog hardware simulator, and expressly teaches logic to perform one or more non-blocking assignments and logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment [*"The non-blocking (<= operator) evaluates all the right-hand sides* for the current time unit *and assigns the left-hand* *sides at the end of the time unit. For example, the following Verilog program ... produces the following output* [program and output omitted for brevity]. " (page 15 of 26, § 2.7.3 Blocking and Non-blocking Procedural Assignments)]. Hyde expressly teaches logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment (*assigns the left-hand sides at the end of the time unit*).

Hyde and Dearth in view of Feinberg in view of Banks are analogous art because all are directed to simulation systems, while Hyde and Dearth in particular are directed to Verilog simulators.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a model that comprises a non-blocking assignment as taught by Hyde in the distributed simulation system of Dearth in view of Feinberg because Hyde expressly teaches that non-blocking assignments "use the old values of the variables at the beginning of the current time unit and to assign the registers new values at the end of the current time unit. This reflects how register transfers occur in some hardware systems" (page 15 of 26, § 2.7.3 Blocking and Non-blocking Procedural Assignments) and therefore enhance the accuracy of simulations of those hardware systems.

Claim 15 recites the method performed by the system of claim 4 and is therefore rejected for the same rationale as claim 4.

Claim 33 recites a system that merely rephrases the limitations of claim 4 and is therefore rejected for the same rationale as claim 4.

5. Claims 23-27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dearth in view of Hyde.

Regarding claim 23, Dearth discloses a computer simulation system (abstract) comprising:

A first model [*"Simulation system 116A can be, for example, the Cadence Verilog hardware simulator... The model within simulation system 116A which represents a simulated circuit is generally in the form of a hardware description language ("HDL") and generally includes data defining input signals to the circuit, output signals of the circuit, internal signals of the circuit (e.g. signals stored in registers), and inter-relationships between the input signals, output signals, and internal signals."* (column 6, lines 49-59)]; and

A first code sequence comprising instructions executable to sample output signals and drive input signals of a second model [*"In FIG. 4, DSP 112A both drives and samples line 414 of bus 214 (FIG. 2)."* (column 8, lines 45-46); also (column 7, lines 1-19); *"VBS 114A stores in resolved output register 406 a simulated signal represented by the data received from resolved 302... VBS 114A drives the resolved signal on line 414 within simulation system 116A. In VBS*

114A, the resolved signal stored in resolved output register 406 is applied to the input of output buffer 408." (column 8, lines 26-44); etc.].

Dearth does not expressly disclose that the model comprises a representation of logic to perform a non-blocking assignment and logic to schedule a call of at least the first code sequence responsive to the non-blocking assignment.

Hyde teaches the capabilities of the Verilog hardware simulator, and expressly teaches logic to perform one or more non-blocking assignments and logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment [*"The non-blocking (<= operator) evaluates all the right-hand sides* for the current time unit *and assigns the left-hand sides at the end of the time unit. For example, the following Verilog program ... produces the following output* [program and output omitted for brevity]. " (page 15 of 26, § 2.7.3 Blocking and Non-blocking Procedural Assignments)]. Hyde expressly teaches logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment (*assigns the left-hand sides at the end of the time unit*).

Hyde and Dearth are analogous art because all are directed to simulation systems, in particular are directed to Verilog simulators.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a model that comprises a non-blocking assignment as taught by

Hyde in the distributed simulation system of Dearth Hyde expressly teaches that non-blocking assignments "use the old values of the variables at the beginning of the current time unit and to assign the registers new values at the end of the current time unit. This reflects how register transfers occur in some hardware systems" (Hyde, page 15 of 26, § 2.7.3 Blocking and Non-blocking Procedural Assignments) and therefore enhance the accuracy of simulations of those hardware systems. In particular, Dearth is particularly concerned with register transfers in Verilog models (Dearth, column 8, lines 26-44; column 6, lines 53-67) while Hyde expressly teaches that non-blocking assignments reflects how register transfers occur in some hardware systems.

Regarding claim 24, Hyde expressly teaches a code sequence that further includes instructions executable to trigger the non-blocking assignment [for example, *"A <= A + 1"* (page 15 of 26, § 2.7.3 Blocking and Non-blocking Procedural Assignments)].

Regarding claim 25, Dearth expressly teaches that a first code sequence includes instructions executable to trigger sampling signals and for driving signals [*"In FIG. 4, DSP 112A both drives and samples line 414 of bus 214 (FIG. 2)."* (column 8, lines 45-46); also (column 7, lines 1-19); *"VBS 114A stores in resolved output register 406 a simulated signal represented by the data received from resolved 302... VBS 114A drives the resolved signal on line 414 within simulation system 116A. In VBS 114A, the resolved signal stored in resolved output register 406 is applied to the input of output buffer 408."* (column 8, lines 26-44); etc.].

Regarding claim 26, Dearth expressly teaches that the first model includes a representation of logic configured to call a first code sequence responsive to a sample clock edge [*"Simulated time is kept by simulation system 116A (FIG. 1) and represents time elapsing during operation of the circuit simulated by simulation system 116A... After a delay 712 (FIG. 7) after rising edge 710 of simulated clock signal CLOCK, i.e., at resolve time 702A, posting by VBS 114A (FIG. 4) is initiated."* (column 10, lines 31-44)].

Regarding claim 27, Dearth expressly teaches that the first model includes a representation of logic configured to schedule a call of a first code sequence responsive to a timestep function [*"Simulated time is kept by simulation system 116A (FIG. 1) and represents time elapsing during operation of the circuit simulated by simulation system 116A... After a delay 712 (FIG. 7) after rising edge 710 of simulated clock signal CLOCK, i.e., at resolve time 702A, posting by VBS 114A (FIG. 4) is initiated."* (column 10, lines 31-44)]. A clock signal is a timestep function.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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